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(Residential Autonomous College affiliated to University of Calcutta)

B.A./B.Sc. FIRST SEMESTER EXAMINATION, MARCH 2021

FIRST YEAR [BATCH 2020-23]

Date : 26/03/2021 **COMPUTER SCIENCE [HONOURS]**

Time : 11.00 am – 1.00 pm **Paper : II [CC 2]** Full Marks : 50

Answer **any five** questions of the following : [5×10]

1. a) A three variable truth table has high output for the following input conditions: 110, 010, 100 and 111. Find the Boolean expression and the corresponding logic circuit using basic gates.

   b) State why NAND and NOR gates are called universal gates. Implement NAND using NOR gates.

   c) Simplify $\overline{AB} + \bar{A} + AB$. Design a logic circuit, using only NAND gates, which has three inputs and gives high output only when all the inputs are equal. [3+(2+1)+(1+3)]

2. a) What do you mean by multiplexer? Cascade few 4-to-1 MUX (e.g., IC 74153) to obtain an equivalent 16-to-1 MUX.

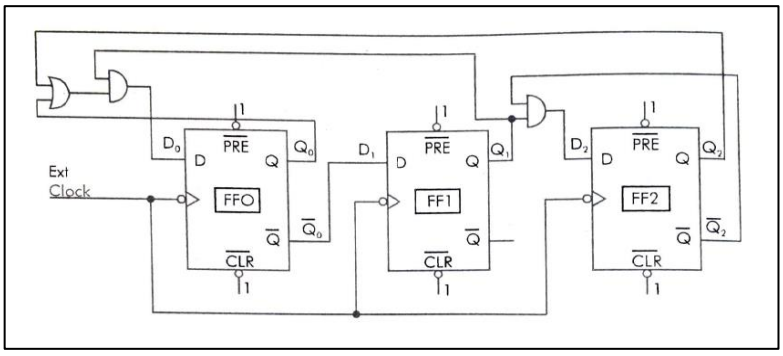
   b) Realize the function F = ∑m(1,3,5,6) using 4-to-1 MUX. Show how the function F(A,B) $A \oplus B$ can be realized using 2-to-1 MUX.

   c) Design a 2-to-4 decoder using basic gates. [(1+3)+(2.5+1.5)+2]

3. a) What do you mean by race-around condition and how can it be resolved?

   b) Design a 1-to-8 ripple counter using edge-triggered JK flip-flops and obtain the count sequence.

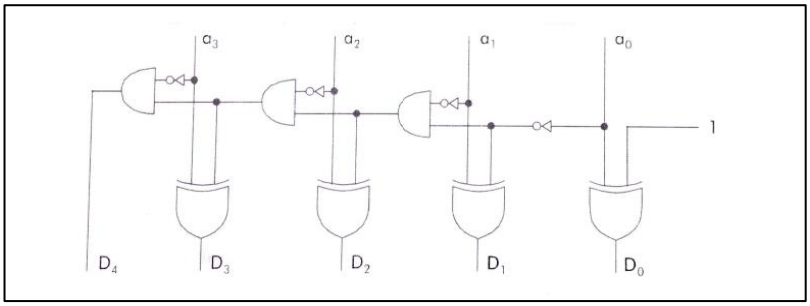
   c) State the advantages of synchronous counter over asynchronous counter. For the following counter circuit obtain the count sequence:



[(1+2)+3+(1+3)]

4. a) Design a shift register which can shift data for all possible ways of shifting data serially and parallely and combination of them. Compare data shifting speeds for all of the configurations.

   b) Design a full-subtractor circuit using full-adder block. Determine the mathematical operation which can be realized by the following circuit, where $a_3a_2a_1a_0$ is the input and $D_3D_2D_1D_0$ is the output:



c) Design a 6-bit Gray-to-Binary code convertor using all full-adder blocks. Use IC 74283 for designing a BCD-to-9's Complement code convertor. [(3+1)+2+(2+2)]

5. a) What is DAC? Explain the principle of working of a weighted resistor DAC. What is the disadvantage of it and how is it resolved in a ladder type DAC?

   b) State the advantages and disadvantages of "Register addressing" mode and "Stack addressing" mode. [(1+3+2)+(1+3)]

6. a) State different methods of memory accessing mechanisms.

   b) State the disadvantages of using Direct mapping function of main memory blocks into cache lines.

   c) Write down the differences in between the followings:

      i) Hardwired controlled CU, Micro Programmed controlled CU

      ii) Von Neumann architecture, Harvard architecture [4+2+(2+2)]

7. a) When a DMA module takes control of a bus, and while it retains control of the bus, what does the processor do?

   b) State the issues in the context of designing "Interrupt-Driven I/O".

   c) Write zero-,one-,two-,and three-address instructions to compute X = (A + B * C)/(D - E * F).

   d) What is Tri-state device? [3+2+4+1]

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